IDEC Chip Design Contest

Design of A Reconfigurable SAR/SS Analog to Digital Converter with Jump Search Algorithm

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Introduction

This paper proposes an ADC that applies jump-search algorithm to a reconfigurable SAR/SS ADC structure for bio signal processing. The hybrid structure is designed by applying the conventional SAR ADC logic to the upper bits and linearly applying voltages corresponding to the lower bits of SS to dummy capacitors. The proposed ADC is also designed to allow for the selection of 12-bit and 14-bit resolutions using external input signals.

Top Cell & Layout

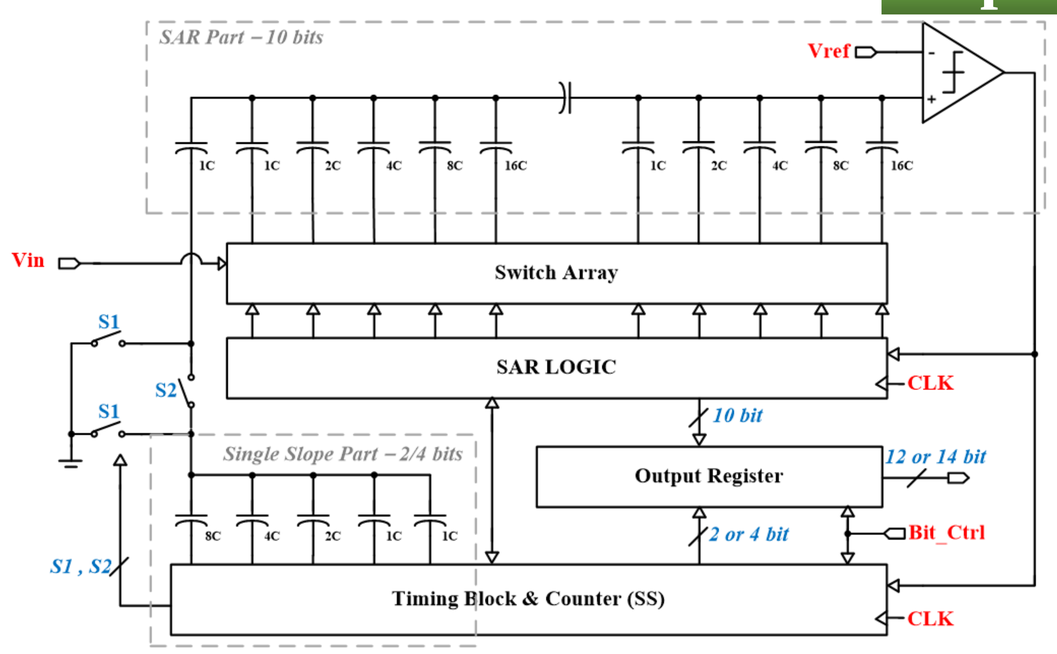

Fig. 1. Block diagram of the proposed 12-14 SAR/SS ADC

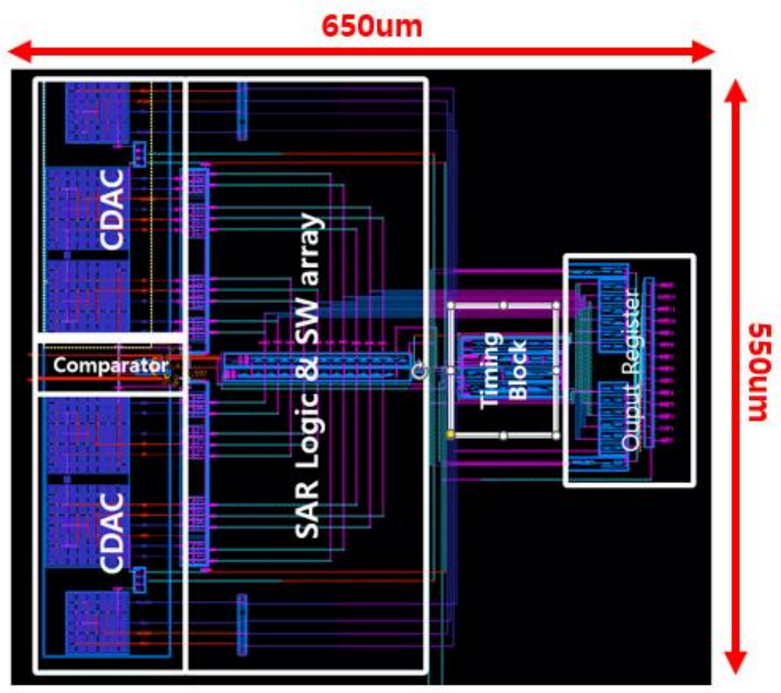

Fig. 2. Proposed ADC Layout

Measurement result & Description

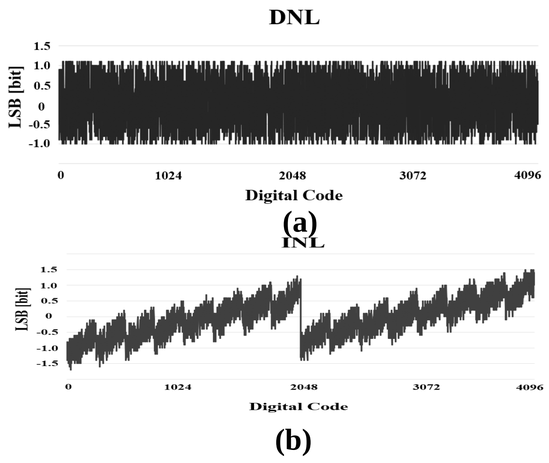

Fig. 3. (a)DNL, (b)INL

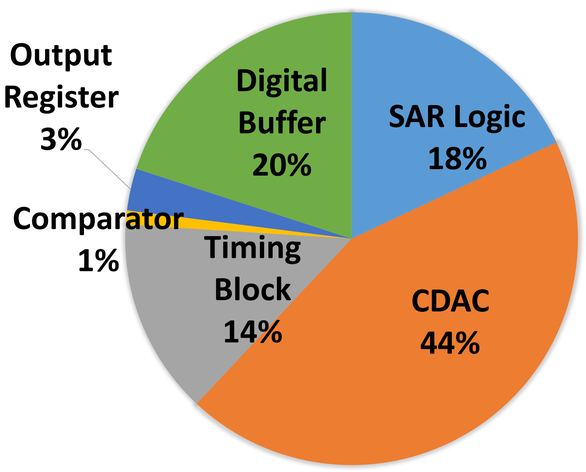

Fig. 4. Power Consumption

In 12-bit mode, after receiving an external analog input signal and converting 10 bits to SAR ADC, the remaining two bits receive output of the binary counter to implement a digital lamp function.

In the 14-bit mode, the jump search algorithm is applied, so the top 2 bits of the SS ADC are converted and stored first, followed by the conversion of the lower 2 bits.

Table 1. Chip Measurement Result

Parameter	This work	
Process	28nm	
Architecture	SAR-SS	
Supply Voltage[V]	1	
Resolution [bit]	12	14
SNDR [dB]	65.8	71.2
ENoB [bit]	10.6	11.5
Sampling rate[S/s]	588k	454k
DNL [bit]	-1.1/1	-1.2/1.1
INL [bit]	-1.7/1.5	-1.8/1.7
Power [uW]	15.1	18.1
FoM* [fJ/step]	16.5	13.8

*FoM = [Power] / ([Sampling rate] × 2^[Resolution])

Table 2. Reconfigurable ADC bit

Bit_Ctrl	SAR bit	SS bit	Total bit
0	10	2	12
1	10	4	14

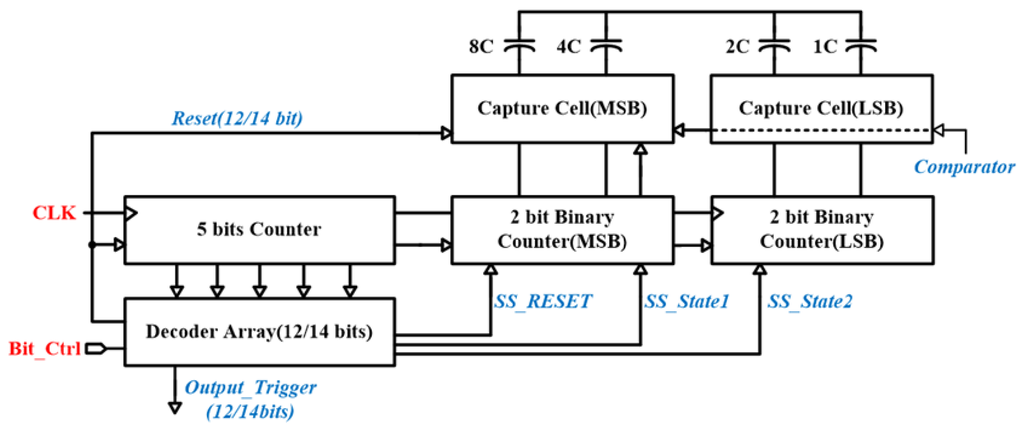

Fig. 5. Timing Block of proposed ADC

Conclusion

This circuit is designed a reconfigurable ADC structure using Timing block. In the 14-bit mode, the bits were converted using the jump search algorithm, so it can quickly find the bit detection of SS.
Lastly, additional capacitors were added to dummy capacitors to reduce the number of capacitors used in C-DAC.
The ADC was implemented using CMOS 28nm process and 1-poly 8-metal. Layout Area is 650um X 550um, Supply voltage is 1V.

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